CLAIMS

I claim:

1. A method of manufacturing a semiconductor device comprising:

providing a semiconductor substrate having first and second main surfaces opposite to each other, the semiconductor substrate having a heavily doped region of a first conductivity type at the second main surface and having a lightly doped region of the first conductivity type at the first main surface;

providing in the semiconductor substrate a plurality of trenches and a plurality of mesas with each mesa having an adjoining trench and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position, at least one mesa having a first sidewall surface and a second sidewall surface, each of the plurality of trenches having a bottom;

doping with a dopant of a second conductivity type the first sidewall surface of the at least one mesa to form a first doped region of the second conductivity type;

doping with the dopant of the second conductivity type the second sidewall surface of the at least one mesa to form a second doped region of the second conductivity type;

doping with a dopant of the first conductivity type the first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall, and doping with the dopant of the first conductivity type the second sidewall surface of the at least one mesa to provide a fourth doped region of the first conductivity type at the second sidewall;

lining at least the trenches adjacent to the at least one mesa with an oxide material; and

filling at least the trenches adjacent to the at least one mesa with one of a semi-insulating material and an insulating material.

2. The method according to claim 1, wherein the oxide lining is formed by one of low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) and a spun-on-glass (SOG) deposition.

3. The method according to claim 1, further comprising:

forming a layer of undoped polysilicon, after the oxide lining step, over the trench bottoms and the mesas, each including the first and second sidewalls.

4. The method according to claim 1, wherein the step of filling the plurality of trenches with one of a semi-insulating material and an insulating material includes filling the plurality of trenches with at least one of undoped polysilicon, doped polysilicon, doped oxide, undoped oxide, silicon nitride and semi-insulating polycrystalline silicon (SIPOS).

5. The method according to claim 1, wherein the first sidewall surface has a first predetermined inclination maintained relative to the first main surface and the second sidewall surface has a second predetermined inclination maintained relative to the first main surface.

6. The method according to claim 1, wherein the first and second sidewall surfaces are generally perpendicular relative to the first main surface.

7. The method according to claim 1, wherein the plurality of trenches are formed utilizing one or more of plasma etching, reactive ion etching (RIE), sputter etching, vapor phase etching and chemical etching.

8. The method according to claim 1, wherein the implanting of the dopant of a second conductivity type into the first sidewall surface is performed at a first predetermined angle of implant.

9. The method according to claim 1, wherein the doping with the dopant of a second conductivity type into the second sidewall surface is performed at a second predetermined angle of implant.

10. The method according to claim 1, wherein the doping with the dopant of the first conductivity type into the first sidewall surface is performed at the first predetermined angle of implant.

11. The method according to claim 1, wherein the doping with the dopant of the first conductivity type into the second sidewall surface is performed at the second predetermined angle of implant.

12. The method according to claim 1, further comprising:

diffusing the dopants of the second conductivity type into the at least one mesa prior to doping with the dopants of the first conductivity type.

13. A semiconductor formed by the method of claim 1.

14. A method of manufacturing a semiconductor device comprising:

providing a semiconductor substrate having first and second main surfaces opposite to each other, the semiconductor substrate having a heavily doped region of a first conductivity type at the second main surface and having a lightly doped region of the first conductivity type at the first main surface;

providing in the semiconductor substrate a plurality of trenches and a plurality of mesas, with each mesa having an adjoining trench and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position, at least one mesa having a first sidewall surface and a second sidewall surface, each of the plurality of trenches having a bottom;

doping with a dopant of the first conductivity type the first sidewall surface of the at least one mesa to form a first doped region of the first conductivity type;

doping with a dopant of the first conductivity type the second sidewall surface of the at least one mesa to form a second doped region of the first conductivity type;

doping with a dopant of the second conductivity type the first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall, doping with the dopant of the second conductivity type the second sidewall of the at least one mesa;

lining at least the trenches adjacent to the at least one mesa with an oxide material; and

filling at least the trenches adjacent to the at least one mesa with one of a semi-insulating material and an insulating material.

15. The method according to claim 14, wherein the oxide lining is formed by one of low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) and a spun-on-glass (SOG) deposition.

16. The method according to claim 14, further comprising:

forming a layer of undoped polysilicon, after the oxide lining step, over the trench bottoms and the mesas, each including the first and second sidewalls.

17. The method according to claim 14, wherein the step of filling the plurality of trenches with one of a semi-insulating material and an insulating material includes filling the plurality of trenches with at least one of undoped polysilicon, doped polysilicon, doped oxide, undoped oxide, silicon nitride and semi-insulating polycrystalline silicon (SIPOS).

18. The method according to claim 14, wherein the first sidewall surface has a first predetermined inclination maintained relative to the first main surface and the second sidewall surface has a second predetermined inclination maintained relative to the first main surface.

19. The method according to claim 14, wherein the first and second sidewall surfaces are generally perpendicular relative to the first main surface.

20. The method according to claim 14, wherein the plurality of trenches are formed utilizing one or more of plasma etching, reactive ion etching (RIE), sputter etching, vapor phase etching and chemical etching.

21. The method according to claim 14, wherein the doping with the dopant of a second conductivity type of the first sidewall surface is performed at a first predetermined angle of implant.

22. The method according to claim 14, wherein the doping with the dopant of a second conductivity type of the second sidewall surface is performed at a second predetermined angle of implant.

23. The method according to claim 14, wherein the doping with the dopant of the first conductivity type of the first sidewall surface is performed at the first predetermined angle of implant.

24. The method according to claim 14, wherein the doping with the dopant of the first conductivity type of the second sidewall surface is performed at the second predetermined angle of implant.

25. The method according to claim 14, further comprising:

diffusing the implanted dopants of the second conductivity type into the at least one mesa prior to implanting the dopants of the first conductivity type.

26. A semiconductor formed by the method of claim 14.